An Attitude Determination System Implementation to Low Orbit Small Satellite with Fault-Tolerant Techniques

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8th IAA Symposium on Small Satellites for Earth Observation
Summary

- Introduction
- The Attitude Determination System
- The Fault-tolerance Strategy
- Fault-tolerant Architecture
- Detection, Reconfiguration and Recovery Cases
- The Validation Approach
- Conclusions
Introduction

- **UNIESPAÇO Program**
  - Encourage the research and the development of aerospace technology in Brazilian Universities.
  - Enable the training of young researchers in the Aerospace Engineering field.

- **Brazilian Spatial Agency (AEB) – INPE**
  São Paulo – Brazil
Introduction

- **GOAL:** to design a low cost fault tolerant satellite attitude determination system.

- **The top-down approach:**
  - Use of COTS devices: little or no fault tolerance mechanisms at all;
  - Global monitoring scheme that provides fault tolerance to the whole system.
The Attitude Determination System

- **Attitude**
  - Orientation in Space

- **Attitude Determination**
  - Point toward a target
  - Computation
  - Inercial Reference
The Attitude Determination System

Relationships

MAIN SATELLITE SUBSYSTEMS

- ADS – Attitude Determin. System
- ACS – Attitude Control System
- OBS – On-board Computer
- TCS – Telemetry and Command
- COM – Communication System
- PRO – Propulsion System
- POW – Power Control System

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The Attitude Determination System

General Attitude Determination System

ALGORITHM used:
- QUEST (Quaternions Estimator);
- Requires at least: 2 referential points

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SOME DETAILS

ADS (Attitude Determination System)

- Micro-processor PIC24FJ64GA004
  low cost, 16bits, + dedicated 16bits multiplier, encapsuling DIP easy to prototype and mount protoboards
- 3X solid state magnetometer HMC2003
- PSD Hamamatsu
ALGORITHMS TESTED

ADS (Attitude Determination System)

-3 algorithms tested: TRIAD, QUEST, Q-Method (Davenport)

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>CPU Time</th>
<th>Clock cycles</th>
<th>Program memory</th>
<th>Data memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q-método</td>
<td>113.6 ms</td>
<td>567,809</td>
<td>7109 Bytes</td>
<td>338 Bytes</td>
</tr>
<tr>
<td>QUEST</td>
<td>70.8 ms</td>
<td>353,959</td>
<td>6792 Bytes</td>
<td>350 Bytes</td>
</tr>
<tr>
<td>TRIAD(magn.)</td>
<td>69.4 ms</td>
<td>347,024</td>
<td>5940 Bytes</td>
<td>338 Bytes</td>
</tr>
<tr>
<td>TRIAD (sol)</td>
<td>69.3 ms</td>
<td>346,661</td>
<td>5940 Bytes</td>
<td>338 Bytes</td>
</tr>
</tbody>
</table>

-QUEST chosen: CPU, memory, cycles, and robustness, stability and accuracy
The Attitude Determination System
Mission Requirements

- The satellite is planned to work correctly during 2 years.
- Satellite mission: Data collecting
- Low Earth Orbit
- Main functional requirements:
  - Time frame: 1 second;
  - Attitude determination accuracy: 0.5 degree (~ 40 Km)
  - Maximum power allowed: not provided, but should be as minimum as possible;
  - Reliability: 0.96 for a two years mission.
  - Reduced dimensions;

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The Fault-tolerance Strategy

- Fault tolerance is accomplished by the successful execution of two functions:
  - Error and/or fault detection followed by,
  - Confinement and System recovery.

- Fault Tolerance Hierarchy:
  - Coordinated execution of these functions at both local and global levels.

- Assure different detection mechanisms to each functionality, placed in different COTS devices.
The Fault-tolerance Strategy

- **Redundancy:**
  - Three identical instances (microcontrollers).
  - Specific roles assigned to each instance.
  - Attitude provided after an acceptance test.
  - Re-computing if acceptance test fails.
  - Switching to an alternative instance if failure persists.

- **Diversity:**
  - Multiple different detection mechanisms.
The Fault-tolerance Strategy

Techniques Adopted

- **TMR – Triple Modular Redundancy**
  - Three identical modules programmed with the *same software*.
  - Two of three modules working with well defined roles.

- **Cold-standby spare**
  - The third module stays in a cold-standby spare mode.

- **Mutual liveness control ("heartbeats exchange")**

- **Recovery Blocks with Acceptation Tests**
  - Temporal technique for re-computing attitude if in error mode.
  - Based on the maximum deviation accepted and the time frame imposed by the system requirements.
Fault-tolerant Architecture

module 1
- magnetometer
- PSD
- microcontroller 1

module 2
- magnetometer
- PSD
- microcontroller 2

module 3
- magnetometer
- PSD
- microcontroller 3

UART 1

UART 2
The Fault-tolerance Architecture
Microcontroller Roles

- **Master mode:**
  - Verifies the Sampler liveness;
  - Stores in its memory the last valid attitude computed.
  - Resets Sampler when it suspects of Sampler’s failure.
  - Awakes the Sleeper after rebooting the Sampler.
  - Judges the validity of the attitude calculated by the Sampler.
  - Decides which value of attitude will be sent out of the system.
  - Provides the last computed value of the attitude stored in his memory as output of the system, when one of the other modules fails and there is no time to re-compute the attitude.
The Fault-tolerance Architecture

Microcontroller Roles

- **Sampler mode:**
  - Reads data from sensors and makes the A/D conversion;
  - Computes the attitude.
  - Stores in his memory the last valid attitude computed to be used only in case of Master’s failure.
  - Verifies the Master liveness.
  - Restarts the microcontroller when it suspects Master’s failure and inherits the Master status.
  - Awakes the Sleeper after rebooting the Master.

- **Sleeper mode:**
  - Remains powered consuming very little energy.
  - Always becomes Sampler when awakened.
Detection, Reconfiguration and Recovery cases
Detection, Reconfiguration and Recovery cases

Timeline 1 represents initialization phase.
Timeline 2 represents A/D conversion.
Timeline 3 represents Attitude Matrix calculation.
Timeline 4 represents attitude data transmission via UART2.
Timeline 5 represents acceptance test.
Timeline 6 represents attitude data transmission via UART1.

Arrows in black color represents heartbeats.
Arrows in red represent attitude.
A heartbeat is sent periodically via UART2.
A heartbeat is waited periodically via UART2.
Detection, Reconfiguration and Recovery cases

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Timeline 6 represents attitude data transmission via UART1.
Timeline 7 represents SAMPLER’s fault suspicion, RESET SAMPLER and wakening SLEEPER to become the new SAMPLER.

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The Validation Approach Experimental System
The Validation Approach Experimental Tests

- **Type of faults injected:**
  - Bit flips, Input glitches, Clock skews and Low power voltage
  - Data Acquisition Board (DAQ – National Instruments)

- **Frequency of injection:**
  - Three random selected faults per second programmed (Labview).

- **Results:**
  - Maximum observed recovery delay: 58 ms (MCUs clock 8 MHz)
  - Attitude computed every 288 ms and serially sent every 400 ms.
VALIDATION PLANNING

- prototype mounted to fly in stratospheric balloon (storing TM)
- mount in cubesat/tubesat like satellite structures
Conclusions

- The results attest that the FT system attends the project requirements.
- Future tests:
  - Realization of radiation ground testing experiments to check the behavior of the system with respect to real faults.
- More tests must be carefully prepared to prove the solution effectiveness.
- The main contribution states on the development of a consistent fault-tolerant strategy based on hardware/software detection mechanism combined to attend the system requirements.
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